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I HEREBY CERTIFY that annexed hereto is a true copy of documents filed in connection with the following patent application:

Application No.	970888
Date of filing	15 December 1997
Applicant	TELLABS RESEARCH LIMITED, an Irish company of Shannon Industrial Estate, Shannon, County Clare, Ireland.

Dated this 12TH day of June 2000.

Gerard Barrett

An officer authorised by the
Controller of Patents, Designs and Trademarks.

FORM NO. 1

REQUEST FOR THE GRANT OF A PATENT

PATENTS ACT, 1992

The Applicant(s) named herein hereby request(s)

_______ the grant of a patent under Part II of the Act

__X__ the grant of a short-term patent under Part III of the Act

on the basis of the information furnished hereunder.

1. Applicant(s)

Name

TELLABS RESEARCH LIMITED

Address

Shannon Industrial Estate
Shannon
County Clare
Ireland

Description/Nationality

An Irish Company

2. Title of Invention

"An ATM Cell Processor"

3. Declaration of Priority on basis of previously filed application(s) for same invention (Sections 25 & 26)

Previous filing date	Country in or for which filed	Filing No.
December 15, 1997	Ireland	970888

4. Identification of Inventor(s)
Name(s) of person(s) believed
by Applicants(s) to be the inventor(s)

Kevin Dewar, a British subject of Stone Park, Ballyallia, Ennis, County Clare, Ireland

Brendan O'Dowd an Irish citizen of 4 Ashmount, Raheen, Limerick, Ireland

Gavin Brebner, a British Subject of 73 Chemin Charriere Blanche, 69130 Emily, France

5. Statement of right to be granted a patent (Section 17(2) (b)

By virtue of an Assignment dated December 3, 1997

6. Items accompanying this Request – tick as appropriate

(i) X prescribed filing fee (£50.00)

(ii) X specification containing a description and claims

_____ specification containing a description only

X Drawings referred to in description or claims

(iii) X An abstract

(iv) _____ Copy of previous application (s) whose priority is claimed

(v) _____ Translation of previous application whose priority is claimed

(vi) X Authorisation of Agent (this may be given at 8 below if this Request is signed by the Applicant (s)

7. Divisional Application (s)

The following information is applicable to the present application which is made under Section 24 –

Earlier Application No: ....

Filing Date: ....

8. Agent

The following is authorised to act as agent in all proceedings connected with the obtaining of a patent to which this request relates and in relation to any patent granted -

Name	Address
John A. O'Brien & Associates	The address recorded for the time being in the Register of Patent Agents, and currently Third Floor, Duncairn House, 14 Carysfort Avenue, Blackrock, Co. Dublin, Ireland.

9. Address for Service (if different from that at 8)

As above

Signed ____________________ John A. O'Brien & Associates

Date August 31, 1998

"An ATM Cell Processor"

The invention relates to a processor for handling asynchronous transfer mode (ATM) cells. An object of the invention is to provide for efficient handling of cells by a processor. Another object is that the processor has flexibility in the manner in which it operates so that it may be used in different environments with relatively simple configuration.

A still further object is to provide a cell processor which may be controlled in a comprehensive manner with relatively simple control circuits.

According to the invention, there is provided an ATM cell processor comprising at least two interfaces, and a queueing function between the interfaces for controlling transfer of cells. The queueing function allows cell traffic management in a very effective manner. The interfaces are preferably bi-directional.

Preferably, the queueing function uses a cell memory for storage of cell queues, and a control memory for storing queueing control settings. This is a very effective way of achieving the necessary control in a flexible manner.

In one embodiment, the memory is at least partly external to the processor and is accessed via a controller. This allows easy expansion and flexibility for different applications generally.

In another embodiment, the processor further comprises a mapping function for mapping received cells from a line according to the VPI/VCI. This allows integration of the processor into a system having multiple internal destinations for received cells.

Preferably, the mapping function comprises means for adding an additional header for internal control signalling. This further enhances effectiveness of internal routing of signals.

In one embodiment, the processor further comprises a policing function for monitoring traffic characteristics of cells received from the line. This is very important for connection of a system with multiple client systems and is particularly useful for monitoring contracts.

In one embodiment, the processor further comprises a segmentation and reassembly (SAR) interface for handling ATM cell control signals. This allows connection of the cell processor to a control processor in an efficient manner using ATM cells for control signalling. Thus the cell processor may be easily configured for a wide range of applications – the control processor performing initialisation and on-line control and monitoring functions.

In one embodiment, the SAR interface is connected to the queueing function. This allows flexible management of control signal flow according to suitable priority queuing schemes.

In another embodiment, the cell processor comprises a control processor interface connected to a memory controller to allow initial setup configuration and on-going monitoring.

The invention will be more clearly understood from the following description of some embodiments thereof, given by way of example only with reference to the accompanying drawings in which:-

Fig. 1 is a schematic representation of a cell processor of the invention;

Fig. 2 is a diagram illustrating operation of a queue server matrix; and

Fig. 3 is a diagram illustrating a UTOPIA interface.

Referring to Fig. 1, there is shown a cell processor 10 of the invention. The processor 10 is an application specific integrated circuit (ASIC), the application being processing of ATM cells.

The main components of the processor 10 are now briefly described briefly with reference to general signal flows through the processor. The cell rate handled is 373 K cells per second, which represents a bit rate of greater than 155 Mpps. The processor 10 has a backplane interface 11 for interfacing according to the CUBIT™ protocol via a backplane. The backplane interface 11 may thus be used for interfacing where the cell rate is not well controlled. This problem is overcome with traffic management performed by a queueing function 12. The queueing function 12 is very important as it performs extensive buffering operations using DRAM or SRAM external to the processor 10 and accessed via a controller 13. It also uses an SRAM controller 14 for access to additional off-chip SRAM. The off-chip memory is used in general for such things as manipulating link lists, and storing cells awaiting transfer. More specifically, the SRAM accessed by the controller 14 is used effectively as an external register and to store data including the queue sizes. On the other hand, the DRAM or SRAM accessed via the controller 13 (Cell RAM) is used for storing actual cells. When dequeueing from the Cell RAM, the SRAM is used to track the cells using pointer information.

Continuing on the path A indicated in Fig. 1, the cells are then transferred to a multi-PHY line interface 15. This is a master interface which supports many ports, in this embodiment eight. Again, the UTOPIA protocol is used.

Thus, in the path A, the processor 10 does not change the cells, but does manage output to the line by using queueing mechanisms.

In the opposite direction, cells are received as indicated by the arrow B at the line interface 15 and are transferred to a mapping function 16. The mapping function 16 changes the VCI/VPI headers according to the destination of the cells and by doing this, it re-directs them to the correct destination. The cells are passed to a policing function 17

which operates according to algorithms to evaluate certain policing parameters such as the cell rate for a particular contract. Various parameters are taken into account such as the temporary nature of any usage of excessive bandwidth for a particular contract. The SRAM accessed via the controller 14 is used for some of these functions. After the policing functions, the cells are transferred to the backplane interface 11.

The processor 10 also comprises a processor interface 20 and a configuration and status function 21, which are connected to the queueing function 12 and the SRAM controller 14. This allows a microprocessor to access the processor 10 and perform a limited set of functions including initial setup and configuration and subsequent status monitoring. An important initial setup function is configuration of the SRAM 14. Subsequently, the processor can access the SRAM locations via the controller 14 and the interface 20 to monitor parameters such as the count of dropped cells.

An important aspect of the processor 10 is that it can use control signals communicated in the ATM format. To do this, it uses a segmentation and reassembly (SAR) interface 25 which performs AAL5 segmentation and reassembly of ATM messages. This interface is used for communication of ATM messages with a SAR device. The SAR device interfaces with another device such as a microprocessor (possibly the same microprocessor as is connected to the interface 20) for comprehensive control communication. The ATM nature of the communication is transparent to the microprocessor because of operation of the SAR device. Thus, a single microprocessor may have access to the processor 10 in two different manners, one being a direct access for initial setup and monitoring of parameters, the other being for comprehensive control communication.

In more detail, the cells which are received at the backplane interface 11 are queued in one of the multiple queues depending on their VPI/VCI. The queues are serviced on a pre-programmed basis to implement a priority queueing system. Queues that grow too large may have cells discarded on a configured basis. Statistics are kept on the number of

cells received, the number of cells transmitted, the number of bad cells, and the number of cells dropped due to congestion.

Queueing is initialised by a microprocessor using the configuration and status function 21. This function has registers, in which there is a notional split of registers related to queueing and those related to dequeueing. The queueing function 12 uses a significant number of tables to control the buffering and congestion management functions. One such table is a path descriptor, the start address of which is provided by a configuration register. The VPI of an incoming cell is used to form an offset into this table. In addition there are special path descriptors for mapping, the SAR, and the processor, the addresses again being provided by configuration registers.

Another table is a queue descriptor, which contains information about an individual queue. All queues are identical, however, they may appear to have different priorities depending on programming of a queue server matrix. Queues are irrevocably tied to target output ports and each of the eight line ports has eight queues associated with it. In addition, a single queue is maintained for each of the processor, SAR, and mapping entities. Mapping between queues and targets is specified in two tables, one for each of aggregate and tributary modes. Each queue has a four-word descriptor, and the offset from the value of the configuration register holding the start location is simply the queue number multiplied by four.

The queue server matrix controls the order in which queues are serviced. Its location and maximum size (1024 elements) are indicated by configuration registers. Each element of the matrix holds three words. The three words are to be interpreted as shown in Fig. 2. The twelfth byte is not used. The queues are checked in ascending order, i.e. the first queue checked is the most significant byte of the first word. Within each byte, only the least significant seven bits are meaningful, i.e. bits 6 to 0.

Storage pools of the queues are referred to as heaps, and consist of stacks of DRAM addresses. There are twenty heaps maintained. The heap structure is implemented as a

set of pointers kept internally and also the DRAM addresses which are stored in the SRAM. Initialisation of the heap involves programming up the pointers into SRAM for the top-of-stack and start-of-stack for each used heap, and then initialisation of the SRAM location between those two pointer values with a unique and valid set of DRAM locations. Configuration registers are used for programming the heap pointers.

As shown in Fig. 1, the output cells of the queueing function are transferred to the line interface 15 or the SAR interface 25.

In the opposite direction, cells received at the line interface 15 are passed to the mapping and policing functions 16 and 17. The cells are passed to the backplane interface 11, to the queueing function 12, or are dropped. Again, the configuration registers store the initialisation information. SRAM tables are maintained by the functions 16 and 17. There are five tables associated with the mapping function 16 as follows:

- per port statistics table,

- VCC connection table,

- dequeue connection table, and

- secondary mapping descriptor table.

Storage of these tables is set by the configuration registers. The per port statistics table stores information including the numbers of cells with invalid and disabled VPI/VCIs and with unsupported PTIs. It also includes the VPI/VCIs of the last disabled and invalid cells.

The VCC connection table contains the following information on a per connection basis:-

mapping descriptor.

received cell count,

dropped cell count, and

GCRA words 1 – 4.

The VPC connection table is identical, except that VPIs are used in place of VCIs.

The dequeue connection table has a maximum of 1024 entries and consists of 1024 32 bit mapping descriptors.

The secondary mapping descriptor table consists of 4096 32 bit entries. Each secondary mapping descriptor is 14 bits long, as set out below.

Field Name	Size	Bit Position
Reserved	18	14-31
map_vpi	1	13
cell_routing	3	10-12
vci_map	10	0-9

Referring now to the three UTOPIA interfaces, Fig. 3 shows an overview. All of the interfaces use the appropriate Start-of-Cell (SOC) signal to initialise cell reception from an external source. Each interface counts octets and an error indication is given when a SOC is activated at an unexpected time. This gives a warning of malformed cells entering the ASIC whilst providing a mechanism to recover at the next cell boundary. Short cells are discarded, whilst long cells are truncated and passed on. Both cause an error indication.

The invention is not limited to the embodiments described, but may be varied in construction and detail within the scope of the claims.

Claims

1. An ATM cell processor comprising at least two interfaces, and a queuing function between the interfaces for controlling transfer of cells.

2. A cell processor as claimed in claim 1, wherein the interfaces are bi-directional, and wherein the queuing function uses a cell memory for storage of cell queues, and a control memory for storing queueing control settings, and wherein the memory is at least partly external to the processor and is accessed via a controller, and wherein the processor further comprises a mapping function for mapping received cells from a line according to the VPI/VCI, and wherein the mapping function comprises means for adding an additional header for internal control signalling.

3. A cell processor as claimed in claims 1 or 2, further comprising a policing function for monitoring traffic characteristics of cells received from the line.

4. A cell processor as claimed in any preceding claim, further comprising a segmentation and reassembly (SAR) interface for handling ATM cell control signals, and wherein the SAR interface is connected to the queueing function, and wherein the processor further comprises a control processor interface connected to a memory controller to allow initial setup configuration and on-going monitoring.

5. A cell processor substantially as described with reference to the drawings.

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~~ABSTRACT~~

~~"An ATM Cell Processor"~~

8 (Fig. 1)

An ATM cell processor (10) has a backplane interface (11), a queuing function (12), and a controller (13). An SRAM controller (14) accesses off-chip RAM. A master interface (15) supports multiple ports. A mapping function (16) changes headers of cells received from the master or line interface(15).

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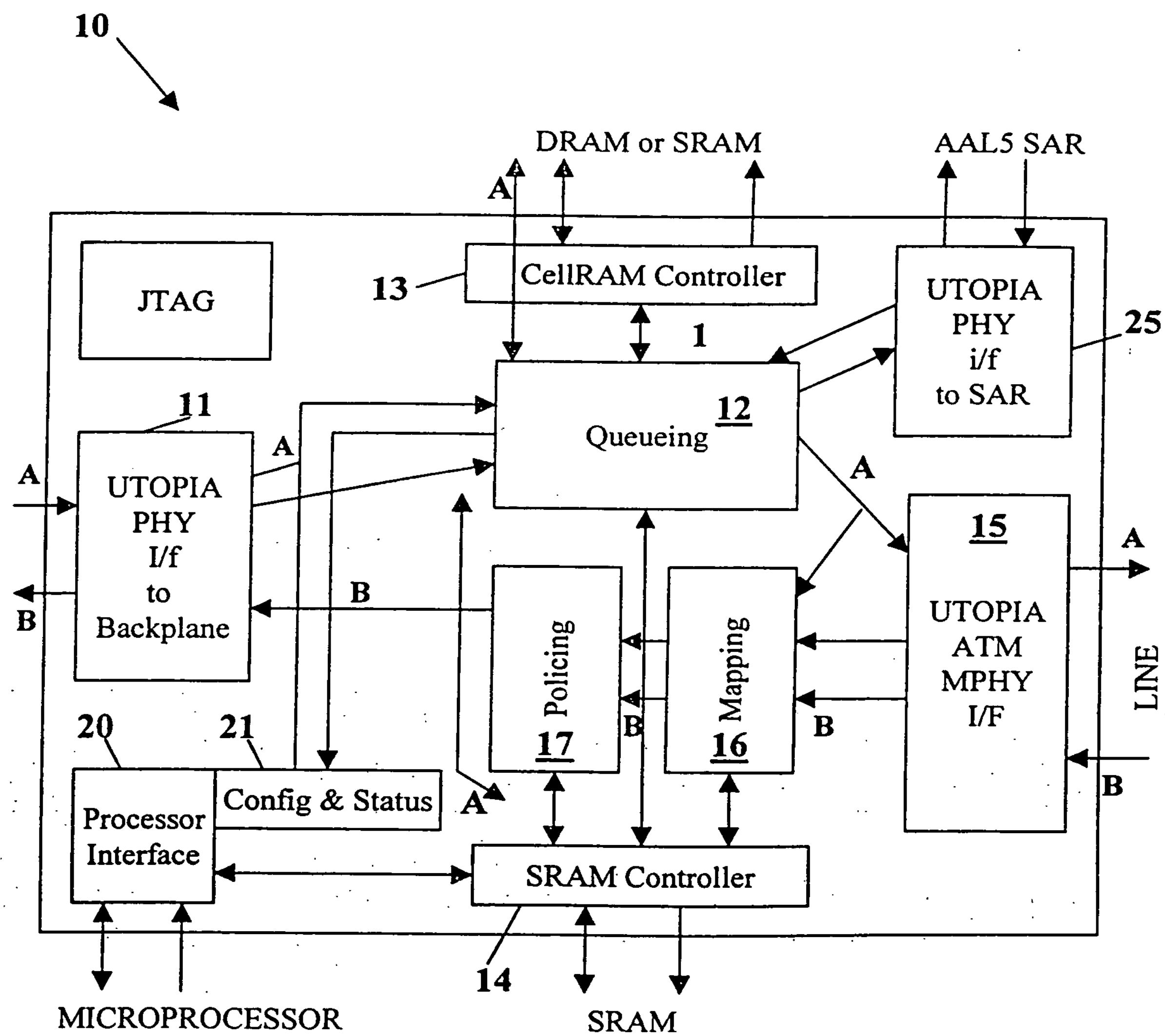
Fig 1



10
DRAM or SRAM
AAL5 SAR
A
JTAG
13
CellRAM Controller
1
UTOPIA PHY i/f to SAR
25
11
A
Queueing
12
A
UTOPIA PHY I/f to Backplane
A
B
B
15
A
UTOPIA ATM MPHY I/F
LINE
Policing
17
Mapping
16
B
B
B
20
21
Config & Status
A
Processor Interface
SRAM Controller
14
MICROPROCESSOR
SRAM

Fig. 1

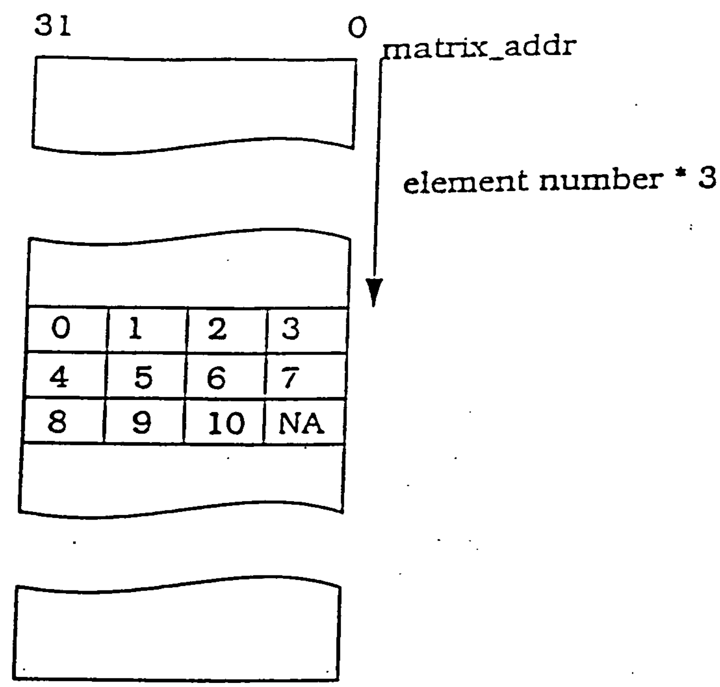


Fig. 2

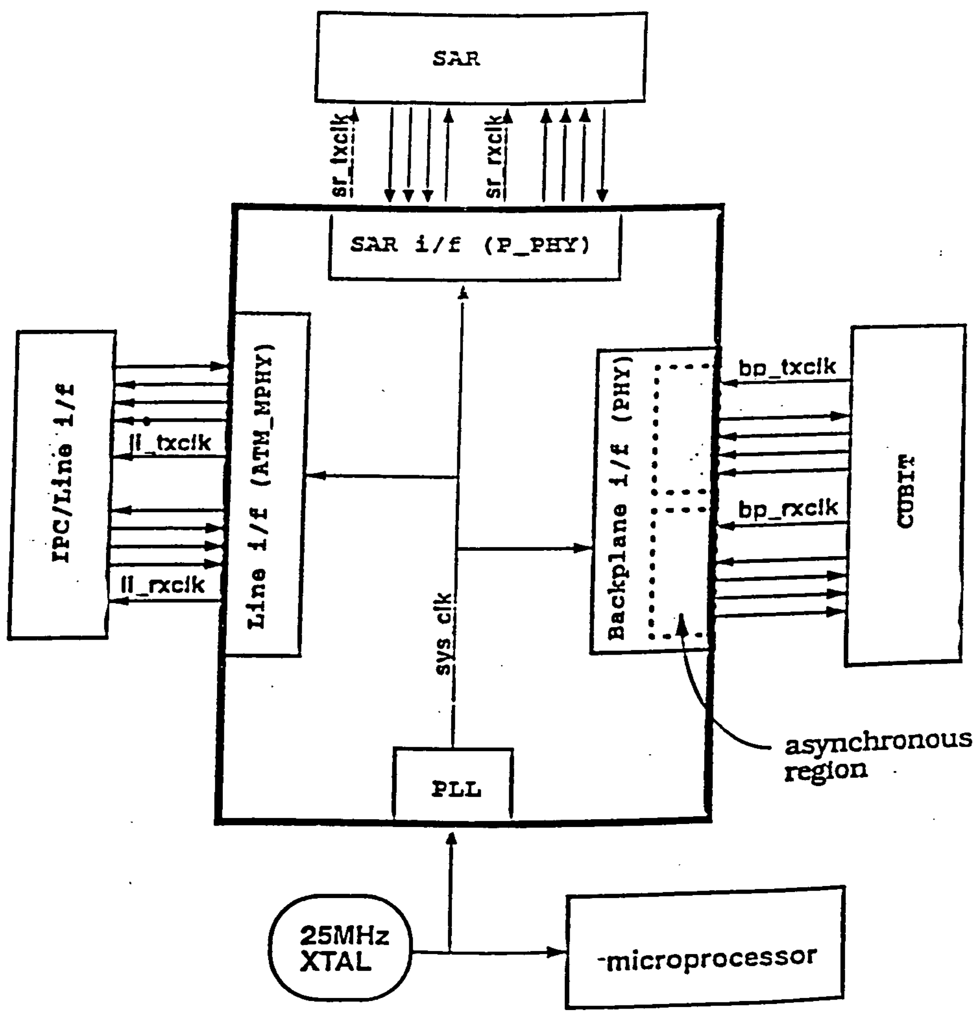

SAR
sr_txclk
sr_rxclk
SAR i/f (P_PHY)
IPC/Line i/f
ll_txclk
ll_rxclk
Line i/f (ATM_MPHY)
Backplane i/f (PHY)
bp_txclk
bp_rxclk
CUBIT
sys_clk
asynchronous region
PLL
25MHz XTAL
microprocessor

Fig. 3